LWO-DAC-B-QSFP-1M

40G DAC Breakout cable, 1xQSFP+(40G) to 4xSFP+(10G), 1m

Features

- Compliant with SFF-8436, SFF-8431, SFF-8432 and SFF-8472
- Up to 10.3125Gbps data rate per channel
- Up to 7m transmission
- Operating temperature: -40°C to +80°C
- Single 3.3V power supply
- RoHS compliant

Applications

- 40G Ethernet

General Description

The 40Gbps QSFP+ to 4x SFP+ Direct Attach Copper (DAC) Breakout Cable is a high-performance, cost-effective connectivity solution designed for short-range interconnections in data centers and enterprise networking environments. It enables a hybrid connection between a single 40G QSFP+ port on a high-speed switch and four individual 10G SFP+ ports on servers, storage devices, or downstream switches, effectively splitting a single 40Gbps channel into four independent 10Gbps data streams.

Constructed with high-quality twinaxial copper cabling and integrated with permanent, factory-terminated transceiver shells on both ends, this passive breakout cable eliminates the need for separate, expensive optical transceivers and fiber patch cords. It operates over short distances—typically ranging from 1 to 7 meters—delivering ultra-low latency, near-zero power consumption, and reliable signal integrity. Fully compliant with SFF-8436, SFF-8431, and IEEE 802.3ba standards, this product offers an ideal plug-and-play solution for high-density network upgrades, top-of-rack (ToR) deployments, and budget-conscious hardware aggregation.

QSFP+ Pin Assignment and Description

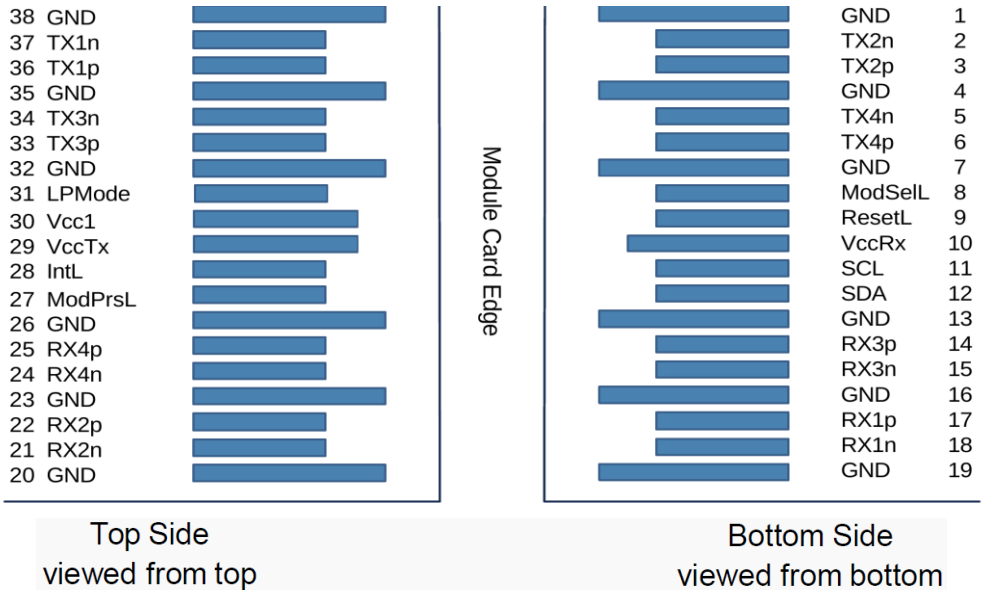

Figure 1: QSFP+ module pad assignment and layout

LWO-DAC-B-QSFP-1M

40G DAC Breakout cable, 1xQSFP+(40G) to 4xSFP+(10G), 1m

PIN Definition

Pad	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	TWI serial interface clock	3	
12	LVCMOS-I/O	SDA	TWI serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL/RxLOS	Interrupt/optional RxLOS	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode/TxDis	Low Power mode/optional TX Disable	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Notes:

1. GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. VccRx, Vcc1 and VccTx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000mA.

LWO-DAC-B-QSFP-1M

40G DAC Breakout cable, 1xQSFP+(40G) to 4xSFP+(10G), 1m

SFP+ Pin Assignment and Description

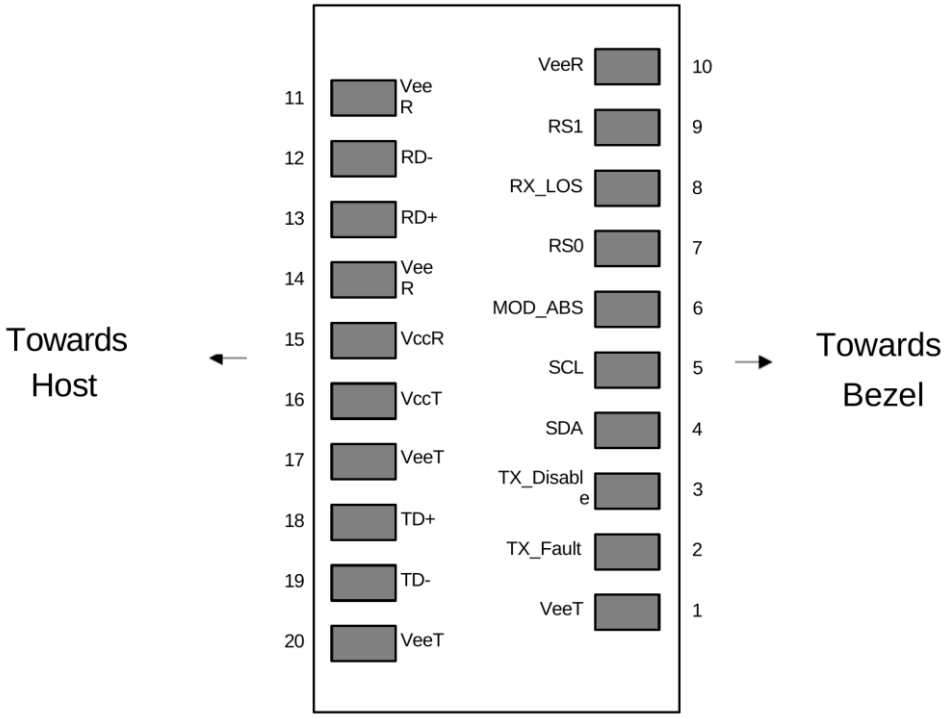

Figure 2: SFP+ module pad assignment and layout

Pad Function Definition

Pin	Logic	Symbol	Name/Description	NOTE
1		VeeT	Transmitter Ground (Common with Receiver Ground)	1
2	LVTTL-O	TX_Fault	Transmitter Fault.	2
3	LVTTL-I	TX_Disable	Transmitter Disable. Laser output disabled on high or open.	3
4	LVTTL-I/O	SDA	2-wire Serial Interface Data Line	4
5	LVTTL-I/O	SCL	2-wire Serial Interface Clock Line	4
6		MOD_ABS	Module Absent. Grounded within the module	4
7	LVTTL-I	RS0	Rate Select 0, internal pull down	5
8	LVTTL-O	LOS	Loss of Signal indication. Logic 0 indicates normal operation.	6
9	LVTTL-I	RS1	Rate Select 1, internal pull down	5
10		VeeR	Receiver Ground (Common with Transmitter Ground)	1
11		VeeR	Receiver Ground (Common with Transmitter Ground)	1
12	CML-O	RD-	Receiver Inverted DATA out. AC Coupled	
13	CML-O	RD+	Receiver Non-inverted DATA out. AC Coupled	
14		VeeR	Receiver Ground (Common with Transmitter Ground)	1
15		VccR	Receiver Power Supply	
16		VccT	Transmitter Power Supply	
17		VeeT	Transmitter Ground (Common with Receiver Ground)	1
18	CML-I	TD+	Transmitter Non-Inverted DATA in. AC Coupled.	
19	CML-I	TD-	Transmitter Inverted DATA in. AC Coupled.	
20		VeeT	Transmitter Ground (Common with Receiver Ground)	1

Notes:

1. Circuit ground is internally isolated from chassis ground.
2. TFAULT is an open collector/drain output, which should be pulled up with a 4.7kΩ ~ 10kΩ resistor on the host board if intended for use. Pull up voltage should be between 2.0V to Vcc + 0.3V. A high output indicates a transmitter fault caused by either the TX bias current or the TX output power exceeding the preset alarm thresholds. A low output indicates normal operation. In the low state, the output is pulled to <0.8V.

LWO-DAC-B-QSFP-1M
40G DAC Breakout cable, 1xQSFP+(40G) to 4xSFP+(10G), 1m

3. Laser output disabled on TDIS>2.0V or open, enabled on TDIS<0.8V.
4. Should be pulled up with 4.7kΩ ~ 10kΩ host board to a voltage between 2.0V and 3.6V. MOD_ABS pulls line low to indicate module is plugged in.
5. Internally pulled down per SFF-8431 Rev 4.1.
6. LOS is open collector output. It should be pulled up with 4.7kΩ ~ 10kΩ on host board to a voltage between 2.0V and 3.6V. Logic 0 indicates normal operation; logic 1 indicates loss of signal.

High Speed Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Differential Impedance	TDR	90	100	110	Ω	
Insertion loss	SDD21	-17.04			dB	At 5.15625 GHz
Differential Return Loss	SDD11			See 1	dB	At 0.05 to 4.1 GHz
	SDD22			See 2	dB	At 4.1 to 11.1 GHz
Differential to common-mode return loss	SCD11			-10	dB	At 0.2 to 11.1 GHz
	SCD22			-10	dB	At 0.2 to 11.1 GHz
Common-mode to common-mode output return loss	SCC11	-3			dB	At 0.01 to 11.1 GHz
	SCC22				dB	At 0.01 to 11.1 GHz

Notes:

1. Reflection Coefficient given by equation SDD11(dB) < -12 + 2 × SQRT(f), with f in GHz.
2. Reflection Coefficient given by equation SDD11(dB) < -6.3 + 13 × log10(f/5.5), with f in GHz.

High Speed Characteristics

The connector is compatible with the SFF-8432 and SFF-8665 specification.

Cable AWG

Length (m)	Cable AWG
1	30
3	30
5	26
7	26

Mechanical Dimensions

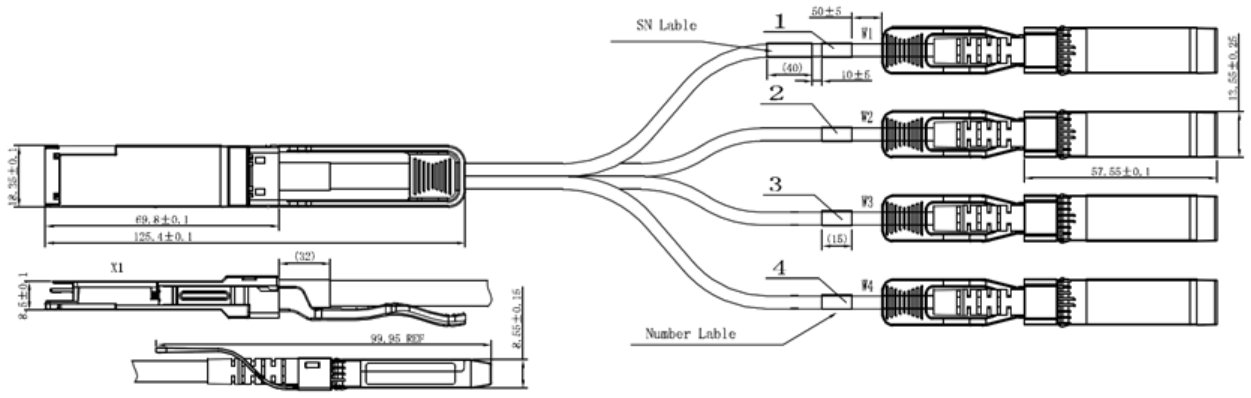

Figure 3. Mechanical Outline

LWO-DAC-B-QSFP-1M

40G DAC Breakout cable, 1xQSFP+(40G) to 4xSFP+(10G), 1m

Regulatory Compliance		
Feature	**Test Method**	**Performance**
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.7	Class 1 (>2000 Volts)
Electromagnetic Interference (EMI)	FCC Class B	Compliant with Standards
Electromagnetic Interference (EMI)	CENELEC EN55022 Class B	Compliant with Standards
Electromagnetic Interference (EMI)	CISPR22 ITE Class B	Compliant with Standards
RF Immunity (RFI)	IEC61000-4-3	Typically Show no Measurable Effect from a 10V/m Field Swept from 80 to 1000MHz
RoHS Compliance	RoHS Directive 2011/65/EU and it's Amendment Directives 6/6	RoHS 6/6 compliant